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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KELD LANGE and GERO BLANKE

Appeal 2008-1668
Application 09/981,784
Technology Center 2600

Decided: July 7, 2008

Before ROBERT E. NAPPI, SCOTT R. BOALICK, and
JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-16 and 19-24. We have jurisdiction under 35 U.S.C. § 6(b). We reverse and enter a new ground of rejection under 37 C.F.R. § 41.50(b).

STATEMENT OF THE CASE

Appellants invented a radio-operated telecommunications system comprising one or more digital signal processors, wherein each of the digital signal processors is configured to perform symbol rate processing and at least a portion of chip rate processing. By having a single processor perform both functions, fewer components are required.[1] Claims 1 and 20 are illustrative:

1. A base station of a radio-operated telecommunications system comprising:

a receiver processing received information; and

one or more digital signal processors, wherein each of said digital signal processors is configured to perform a symbol rate processing and at least parts of a chip rate processing.

20. A digital signal processor comprising:

means for executing symbol rate processing;

means for executing chip rate processing; and

means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing,

wherein the digital signal processor is a single digital processor having the symbol rate processing means, the chip rate processing means and the switching means and wherein the digital signal processor is disposed inside a receiver.

[1] *See generally* Spec. 2:15-4:21.

The Examiner relies on the following prior art references to show unpatentability:

Warty	US 4,827,499	May 2, 1999
Komara	US 6,161,024	Dec. 12, 2000 (filed Oct. 14, 1999)
Subramanian	US 2001/0034227 A1	Oct. 25, 2001 (filed Jan. 29, 2001)
Sriram	US 6,366,606 B1	Apr. 2, 2002 (filed Feb. 4, 1999)
Özlütürk	US 6,366,607 B1	Apr. 2, 2002 (filed May 14, 1998)

1. Claims 1, 3, 6-13, and 19 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Sriram and Özlütürk.
2. Claims 2, 14, and 16 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Sriram, Özlütürk, and Warty.
3. Claims 4, 5, and 15 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Sriram, Özlütürk, Warty, and Komara.
4. Claims 20-24 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Özlütürk and Subramanian.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments which Appellants could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

OPINION

The Rejection Based on Sriram and Özlütürk

We first consider the Examiner's obviousness rejection of claims 1, 3, 6-13, and 19 over Sriram and Özlütürk (Ans. 4-5). In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

Discussing the question of obviousness of a patent that claims a combination of known elements, the Court in *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007) explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.,* 425 U.S. 273 (1976)] and *Anderson's-Black Rock*[*, Inc. v. Pavement Salvage Co.*, 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740. If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a

showing that "there was an apparent reason to combine the known elements in the fashion claimed." *Id.* at 1740-41. Such a showing requires

> some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ. *Id.* at 1741 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

If the Examiner's burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

Regarding independent claims 1 and 9-12, Appellants argue that ordinarily skilled artisans would not have combined the references in the manner suggested by the Examiner absent impermissible hindsight (App. Br. 17; Reply Br. 9-10).

Appellants also argue that the prior art does not suggest a processor performing symbol rate processing and at least a portion of chip rate processing, as claimed. According to Appellants, since the signal in Özlütürk is despread *before* it is input into the signal processor, chip rate processing is therefore not performed by that processor. Rather, Appellants contend, chip rate processing in Özlütürk occurs before the signals reach the processor (App. Br. 18-21). Appellants add that Sriram similarly teaches performing chip rate processing and symbol rate processing in different system components, namely (1) chip rate processing in the correlator co-

processor 12, and (2) symbol rate processing performed by the processor 37 in the receiver 10 (Reply Br. 5-6).

The Examiner contends that since Sriram teaches that symbols are comprised of chips, any device that performs chip rate processing can also be considered to perform symbol rate processing (i.e., Sriram's correlation controller) (Ans. 8-9). The Examiner further contends that it would have been obvious to integrate the functions of Sriram's receiver 10 and co-processor 12. According to the Examiner, such integration would allegedly "be merely a matter of obvious engineering choice" and would eliminate unnecessary circuit components, thus making the receiver circuitry more compact (Ans. 9-10).

The issue before us, then, is whether Appellants have shown that the Examiner erred in finding that the combination of Sriram and Özlütürk teaches or suggests that at least one digital signal processor performs (1) symbol rate processing, *and* (2) at least parts of a chip rate processing as recited in independent claims 1 and 9-12. For the following reasons, we find that Appellants have shown such error.

Since our resolution of this appeal turns on the interpretation of the terms "symbol rate processing" and "chip rate processing," we first construe these terms. According to Appellants' Specification, "chip rate processing" is "essentially a so-called *despreading* (recovery of the original information)…performed which in the CDMA telecommunications system in question is used to re-separate the transmitted information of the different users in the receiver and to assign this information to the different users" (Spec. 5:23-27; emphasis added). The Specification further notes that "symbol rate processing basically comprises the decoding of the received

information" (Spec. 5:29-30).[2] We find these descriptions tantamount to implicit definitions of the terms "symbol rate processing" and "chip rate processing," and we therefore construe the terms accordingly.[3]

With this construction, we turn to the prior art. Sriram discloses a digital receiver 10, preferably implemented on a digital signal processor (DSP), which communicates with an associated correlator co-processor 12 via a co-processor interface 16. The programmable correlation co-processor can perform all correlation functions for the receiver 10 in accordance with correlation parameters generated by the receiver (Sriram, col. 2, ll. 15-39; Fig. 1).

As shown in Figure 2, the correlator co-processor 12 includes a correlation controller 40. To provide the correlations using a minimum of power, the correlation controller can perform requested correlations of the requested chips stored the chip buffer in portions. For example, at 256 chips per symbol, the correlation controller processes each symbol in 32 chip portions. Upon detecting a symbol in the output buffer 38, the receiver 10 then proceeds with symbol rate processing functions (Sriram, col. 4, ll. 28-42; Fig. 2).

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[2] *See also* Reply Br. at 6 ("Chip rate processing, as is known, relates to processing at the chip level *i.e.*, dispreading [sic] information based on users and symbol processing, as is known, relates to processing information at the symbol level *i.e.*, decoding received information.").

[3] *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1321 (Fed. Cir. 2005) (en banc) ("[T]he specification is the single best guide to the meaning of a disputed term, and…acts as a dictionary when it expressly defines terms in the claims or when it defines them by implication.") (internal quotation marks and citations omitted).

Based on this functionality, we agree with Appellants that neither Sriram nor Özlütürk teaches or suggests a digital signal processor that performs both (1) symbol rate processing, *and* (2) at least parts of a chip rate processing as recited in independent claims 1 and 9-12.

First, as Appellants indicate (Reply Br. 5), the correlator co-processor 12 in Sriram performs chip rate processing using, among other things, chip correlator 34 and correlator controller 40 (Sriram, col. 5, ll. 4-26). Furthermore, the receiver 10 in Sriram performs symbol rate processing, namely via its symbol rate processor 37—a processor whose very label describes its function.

In short, different processors in Sriram perform chip rate processing and symbol rate processing, respectively. That said, however, we note that the claim language of independent claims 9 through 12 merely calls for the processor to perform "*at least parts of* a chip rate processing"—a limitation that does not require performing *all* chip rate processing functions on that processor. In this regard, Sriram's receiver 10 includes a correlation parameter generator 35 that generates and transmits parameters to the correlation co-processor 12 whenever correlation functions are needed (Sriram, col. 3, ll. 58-67; col. 4, ll. 11-27). Nevertheless, we do not find that this preliminary parameter generation reasonably comports with any part of "chip rate processing" as claimed in light of Appellants' implicit definition of the term in the Specification—a process that requires despreading. Based on this definition, it is only the correlation co-processor in Sriram that performs chip rate processing or even a portion of such processing.

Thus, even with the somewhat broader recitation in claims 1 and 9-12 regarding chip rate processing, we still do not find that only one processor in

Sriram performs both symbol rate processing and even a portion of chip rate processing.

Özlütürk fares no better in this regard. Özlütürk discloses in Figure 2 a digital spread spectrum communications system comprising a transmitter 27 and receiver 29. In the transmitter, voice and nonvoice signals are encoded into data at various data rates and spread using a complex pseudo-noise (pn) sequence. The resulting spread signals are combined with other spread signals with different codes, mixed with a carrier signal, and transmitted. As a result, the transmission 55 can have multiple channels with different data rates (Özlütürk, col. 3, ll. 7-40; Fig. 2).

At the receiver, the broadband signal is mixed down to an intermediate carrier frequency 59a, 59b, filtered 61, and mixed 63a, 63b with a locally generated pn sequence that matches the conjugate of the transmitted complex code. This technique effectively despreads the original waveforms that were spread by the same code at the transmitter. The data 65a, 65b is then sent to signal processor 67[4] and decoded (Özlütürk, col. 3, ll. 41-53; Fig. 2).

Thus, since despreading (chip rate processing) in Özlütürk occurs *before* the signal reaches the signal processor 67, the signal processor does not perform both symbol rate processing and at least a portion of chip rate processing as claimed. We find unavailing the Examiner's assertion (Ans. 10) that since there are allegedly no channel despreaders in the embodiments

[4] Although numeral 59 is indicated in the text of Özlütürk as corresponding to the signal processor (Özlütürk, col. 3, l. 52), Figure 2 labels the signal processor with numeral 67. Appellants also noted this inconsistency (App. Br. 18). We therefore presume that this inconsistency is a typographical error and that numeral 67 was intended to correspond to the signal processor.

of Figures 2, 12, and 13, both symbol rate processing and chip rate processing are performed at the signal processor. But as Appellants indicate (App. Br. 20), chip rate processing *has already been performed* to the symbols 95_1-95_n entering the processor 157 shown in Figure 12. This fact is amply evidenced by the despreaders 85_1-85_n whose output produces the symbols 95_1-95_n in Figure 11. These despreaders located before the processor are also illustrated in Figure 13.

Nor do we find persuasive the Examiner's reliance (Ans. 9-10) on Özlütürk's carrier offset correction which can be performed either at the chip level or symbol level (Özlütürk, col. 4, ll. 1-14). Even assuming, without deciding, that this offset correction can somehow be considered as constituting at least part of the chip rate processing or symbol rate processing techniques, we nonetheless agree with Appellants (App. Br. 19; Reply Br. 9), that Özlütürk does not teach performing such offset correction at both the chip level *and* the symbol level, let alone in a single processor.

Lastly, we do not agree with the Examiner (Ans. 9-10) that it would have been obvious to ordinarily skilled artisans to integrate the functions of Sriram's receiver 10 and co-processor 12. Indeed, the Examiner's reason to integrate these functions as an alleged obvious engineering design choice is belied by the very teachings of the reference that the Examiner relies upon, namely Sriram.

The fundamental improvement in Sriram is providing a correlator co-processor 12 that is *separate* from the digital receiver 10. The reason why these processors are separate is that the correlation function in digital receivers typically consumes a large amount of power. By separating the correlation function from the receiver, correlations can be performed on

demand: an improvement that, among other things, reduces power consumption (Sriram, col. 1, ll. 15-51). Thus, Sriram, in our view, actually *teaches away* from integrating the functions of Sriram's receiver 10 and co-processor 12.

For the foregoing reasons, Appellants have persuaded us of error in the Examiner's rejection of independent claims 1 and 9-12. Therefore, we will not sustain the Examiner's rejection of those claims, and dependent claims 3, 6-8, 13, and 19 for similar reasons.

The Rejections of Claims 2, 4, 5, and 14-16

Regarding the obviousness rejections of dependent claims 2, 4, 5, and 14-16 (Ans. 6-7), since we find that the disclosures to Warty and Komara do not cure the deficiencies of the other cited references noted above with respect to independent claims 1 and 9-12, the obviousness rejections of (1) claims 2, 14, and 16 over Sriram, Özlütürk, and Warty, and (2) claims 4, 5, and 15 over Sriram, Özlütürk, Warty, and Komara are also not sustained for similar reasons.

The Rejection of Claims 20-24

We now consider the Examiner's obviousness rejection of claims 20-24 over Özlütürk and Subramanian. At the outset, we note that claims 22 and 23 depend from independent claim 1. Consequently, the Examiner's inclusion of these claims in the rejection of independent claim 20 is inconsistent with the rejection of independent claim 1 (based on Sriram and Özlütürk) and therefore improper for this reason alone. Although this error was repeatedly noted by Appellants (App. Br. 23-24; Reply Br. 12-13), the

Examiner did not address the issue in the Answer. Appellants have therefore persuaded us of error in the Examiner's rejection of claims 22 and 23 on this ground alone.

In any event, with respect to independent claim 20, for the reasons noted previously, we disagree with the Examiner's findings regarding Özlütürk as disclosing a digital signal processor that with the capability to perform both chip rate processing and symbol rate processing (Ans. 7).

We also find the Examiner's reliance on Subramanian (Ans. 7, 8, 11, 12) unavailing. Subramanian discloses a configurable spread spectrum communications device in which an external processor device 102 sends configuration information 103 to a configurable communication device 104 via an interface 109 (Subramanian, ¶¶ 0021-23; Fig. 1A). An exemplary implementation of the external processor device 102 is shown Figure 2 in the form of computer system 120a. Significantly, this computer system interfaces with a configurable multiprocessor device (Subramanian, ¶ 0030; Fig. 2). Using the external processor device in conjunction with the configurable device, the user can implement the functions of the flowchart of Figure 3 including, among other things, generating a signal flow path for a desired operation, creating a system dataflow, and mapping a desired operation onto a function-specific computing element (Subramanian, ¶¶ 0035, 0041-42, 0045; Fig. 3).

While the system dataflow can be associated with signal processing functions including despreading, and symbol rate processing (Subramanian, ¶ 0042), the reference simply fails to teach or suggest that these functions would be implemented on a single digital signal processor as claimed. In fact, Subramanian suggests just the opposite in that the algorithms associated

with these functions are associated with distinct processor groups including a chip-rate processor group and a symbol-sequence processor group (Subramanian, ¶ 0042).

Although Subramanian does indicate that the processor used to implement the flowchart steps can be a dedicated DSP processor (Subramanian, ¶ 0077), this dedicated processor is used by the external processor device 102 (*see, e.g.,* processor 204 in computer system 102a of Fig. 2)—not the configurable communication device 104. That is, while the configuration generation capabilities of the external processor device may employ a dedicated digital signal processor, the configurable communication device—the device that actually implements the so-configured chip rate processing and symbol rate processing functions—does not have such a dedicated processor. Nor is there any suggestion in the cited prior art to use such a dedicated processor for both functions.

For the foregoing reasons, Appellants have persuaded us of error in the Examiner's obviousness rejection of independent claim 20 based on Özlütürk and Subramanian. Therefore, we will not sustain the Examiner's rejection of that claim, and dependent claims 21 and 24 for similar reasons.

NEW GROUNDS OF REJECTION UNDER 37 C.F.R. § 41.50(b)

Under 37 C.F.R. § 41.50(b), we enter new grounds of rejection under 35 U.S.C. § 112.

Claims 20, 21, and 24 are Indefinite Under § 112 as Reciting Means-Plus-Function Limitations Whose Corresponding Structure is Insufficiently Described in the Specification.

Claims 20, 21, and 24 are rejected as being indefinite under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which Appellants regard as their invention. Independent claim 20 recites three means-plus-function limitations, namely (1) means for executing symbol rate processing; (2) means for executing chip rate processing; and (3) means for switching over from one means to another.

Under § 112, sixth paragraph, means-plus-function claim language must be construed by "look[ing] to the specification and interpret[ing] that language in light of the corresponding structure, material, or acts described therein, and equivalents thereof, to the extent that the specification provides such disclosure." *In re Donaldson Co., Inc.*, 16 F.3d 1189, 1193 (Fed. Cir. 1994) (en banc). We therefore turn to Appellants' Specification to construe these limitations.

In connection with independent claim 20 in the Summary of the Claimed Subject Matter section of the Brief, Appellants refer to the Figure and page 6, line 26 to page 8, line 4 of the Specification (App. Br. 9). The Figure shows a digital signal processor 12 comprising blocks 13 and 14 labelled "chip rate processing" and "symbol rate processing," respectively. Also, a block labelled "task allocation 15" is within the processor and is connected to both the "chip rate processing" and "symbol rate processing" blocks.

According to the Specification, "[t]he signal processor 12 is *programmed* such that it can perform the…chip rate processing as well as the…symbol rate processing [functions]…The blocks 13, 14 thus represent *program modules* which define the mode of operation of the signal processor 12" (Spec. 7:4-8; emphasis added). Regarding the task allocation function, the Specification indicates that the signal processor 12 is likewise *programmed* for such a function—a function that includes not only control functions, but also switching over between chip rate processing and symbol rate processing (Spec. 7:15-8:3; emphasis added).

Apart from these general statements pertaining to the programming of the signal processor, however, the Specification does not further detail this programming. Such a general description falls well short of disclosing sufficient structure corresponding to the recited means-plus-function limitations.

It is well settled that "for computer-implemented means-plus-function claims where the disclosed structure is a computer programmed to implement an algorithm, the disclosed structure is not the general purpose computer, but rather the special purpose computer programmed to perform the disclosed algorithm." *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1340 (Fed. Cir. 2008) (citations and internal quotation marks omitted). As such, the application must disclose "enough of an algorithm to provide the necessary structure under § 112, ¶ 6"—a disclosure that can be expressed in any understandable terms (e.g., a mathematical formula, in prose, or as a flowchart). *Id.* But "[s]imply reciting 'software' without providing some detail about the means to accomplish the function is not enough." *Id.* at 1341-42.

Here, merely stating that the signal processor is "programmed" to perform the recited functions on page 7 of the Specification, without more, simply fails to describe sufficient structure to accomplish the recited functions of the means-plus-function limitations of claim 20 as required by *Finisar*. Apart from the general statements that the signal processor is programmed such that it can perform the stated functions, neither the Specification nor the drawing discloses any particular algorithm, formula, flowchart, or code to achieve these results. As such, the disclosed programmed signal processor is tantamount to a general purpose computer, not a special purpose computer with sufficient structure that can achieve the desired results. *See id.*

For the foregoing reasons, independent claim 20 is indefinite under § 112, second paragraph. Dependent claims 21 and 24 are likewise indefinite for similar reasons.

DECISION

We have not sustained the Examiner's rejections with respect to any claims on appeal. Therefore, the Examiner's decision rejecting claims 1-16 and 19-24 is reversed. We have, however, entered a new ground of rejection under 37 C.F.R. § 41.50(b) for claims 20, 21, and 24 under 35 U.S.C. § 112, second paragraph.

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b) which provides that "[a] new ground of rejection . . . shall not be considered final for judicial review."

That section provides that the Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the

following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED
37 C.F.R. § 41.50(b)

KIS

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